AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("__") and the language being deleted contains a strikethrough ("—").

LISTING OF CLAIMS

1-35. (Canceled)

36. (Previously Presented) An apparatus for compressing a plurality of input signals comprising:

a plurality of multiplexers arranged in a plurality of rows, wherein multiplexers in a first row have inputs connected to signals defining bits to be compressed and multiplexers of successive rows have inputs connected to outputs of the multiplexers of the preceding row, wherein each successive row of multiplexers comprises fewer multiplexers than the previous row, wherein a first row of multiplexers is arranged so that each multiplexer in the first row has two inputs, which inputs are coupled to adjacent bit positions of the plurality of input signals, and wherein a second row of multiplexers is arranged so that each multiplexer in the second row has two inputs, in which a first of the inputs is coupled to an output of a first aligned multiplexer in the first row and a second of the inputs is coupled to an output of a second multiplexer in the first row, the second multiplexer being two multiplexers away from the first aligned multiplexer, and wherein a third row of multiplexers is arranged so that each multiplexer in the third row has two inputs, in which a first of the inputs is coupled to an output of a second aligned multiplexer in the second row and a second of the inputs is coupled to

an output of a second multiplexer in the second row, the second multiplexer in the second row being four multiplexers away from the second aligned multiplexer; and

control logic for controlling data select input signals for individual select inputs of the plurality of multiplexers such that individual bits of the plurality of bits are shifted varying amounts, the shift amount and the individual select inputs being determined by a mask.

37. (Previously Presented) The apparatus of claim 36, wherein the plurality of multiplexers are arranged in precisely four rows, wherein a fourth row of multiplexers is arranged so that each multiplexer in the fourth row has two inputs, in which a first of the inputs is coupled to an output of a third aligned multiplexer in the third row and a second of the inputs is coupled to an output of a second multiplexer in the third row, the second multiplexer in the second row being eight multiplexers away from the third aligned multiplexer.

38. (Previously Presented) The apparatus of claim 36, wherein the plurality of multiplexers are collectively configured to be capable of shifting individual bits of the plurality of bits by varying amounts based on the contents of the mask, wherein each additional shift value effectively causes a shifted bit to overwrite a bit that is to be unaffected by a subsequent computation.

39. (Previously Presented) The apparatus of claim 38, further comprising compression control logic, the compression control logic configured to control the

control logic to shift individual bits by an amount equal to a number of bit positions, preceding the current bit position, that are to be unaffected by the computation.

[[39]] 40. (Currently Amended) The apparatus of claim 36, wherein the mask is a pixel mask corresponding to a tile of pixels to be displayed on a display.

[[40]] 41. (Currently Amended) The apparatus of claim [[39]] 40, wherein contents of the pixel mask are based on depth information.

[[41]] 42. (Currently Amended) The apparatus of claim 36, wherein groups of the plurality of bits define data values representing an attribute for pixels to be displayed on a display.

[[42]] 43. (Currently Amended) The apparatus of claim [[41]] 42, wherein the attribute is one selected from the group consisting R, G, B, A, U, and V.

[[42]] 44. (Currently Amended) The apparatus of claim 36, wherein the plurality of multiplexers are arranged in a plurality of rows, wherein multiplexers in a first row have inputs connected to plurality of signals, some of which are to be removed through compression, and multiplexers of successive rows have inputs connected to outputs of the multiplexers of the preceding row.

[[43]] 45. (Currently Amended) The apparatus of claim 36, wherein the control logic for controlling data select input signals for the plurality of multiplexers is responsive to a mask that defines positions of the plurality of signals as the inputs of the first row of multiplexers that are to be removed through compression, such that input signals following input signals that are to be removed are shifted into the position of the preceding signals that are to be removed.

[[44]] 46. (Currently Amended) The apparatus of claim 36, wherein the plurality of multiplexers are collectively configured to be capable of shifting individual signals of the plurality of input signals by varying amounts based on the contents of the mask, wherein each additional shift value effectively causes a shifted bit to overwrite a signal position that is to be removed.

[[45]] 47. (Currently Amended) The apparatus of claim [[44]] 46, further comprising compression control logic, the compression control logic configured to control the control logic to shift individual signals by an amount equal to a number of signal positions, preceding the current signal position, that are to be removed.

[[46]] 48. (Currently Amended) The apparatus of claim 36, further comprising logic for compressing a plurality of groups of bits by shifting compressed groups of bits into bit positions that are to be removed during the compression, the logic being responsive to a mask, wherein contents of the mask define variable amounts that the

plurality of bits are shifted during the compression, the logic further comprising a plurality of multiplexers that are individually selectable by select signal lines, such that the groups of bits are shifted by controllably selecting individual ones of the select signal lines.

[[47]] 49. (Currently Amended) The apparatus of claim [[46]] 48, wherein the mask is a pixel mask and the groups of bits to be compressed correspond to attributes associated with pixels to be displayed.

[[48]] 50. (Currently Amended) The apparatus of claim [[46]] 48, wherein each position of the mask defines a shift amount for a group of bits.

[[49]] 51. (Currently Amended) The apparatus of claim [[48]] 50, wherein the content of each position of the mask is a defined by a single bit, and the shift amount for a group of bits is defined by a summation of preceding mask positions whose contents indicate corresponding pixels are not to be affected by a subsequent computation, wherein the positions of the mask are arranged in an order and the preceding mask positions are those that, as ordered, numerically precede the a given position.

[[50]] 52. (Currently Amended) The apparatus of claim [[49]] 51, wherein the arranged order of the positions of the mask is arbitrary.